NML - Master Oscillator

This document presents a general description of the design and performance of the master oscillator for the New Muon Laboratory (NML) International Linear Collider Test Area (ILCTA).

Table of content

1. **Requirements**
    a. **List of clients**

The master oscillator clients are listed below:

- Laser / beam source
- Reference line distribution system
- RF stations
- Timing systems
- Instrumentation
- LO distribution line system
- Monitor systems

b. **List of frequencies with power level**

The master oscillator frequencies are listed below, with the corresponding clients:

- 1313 MHz local oscillator reference
    - LO distribution system
    - RF receivers
    - RF transmitter
    - MFC controller clock
- 1300 MHz RF reference
    - RF reference distribution line system
    - RF receivers reference channel
    - Instrumentation
- 81.25 MHz laser reference
    - Laser system
- 52.00 MHz piezo system LO
    - Piezo cavity resonance control system
- 50.00 MHz ESECON clock
    - VME ESECON controller clock
- 9.027 MHz timing clock system NML-CLOCK
    - VXI Timing reference clock

c. **List of phase noise specifications**

- Phase noise
    - 1313 MHZ
    - 1300 MHz
    - 81.25 MHz
    - 52.00 MHz
    - 50 MHz
    - 9.025 MHz

- Signal levels
  - 1313 MHz +10 dBm
  - 1300 MHz +10 dBm
  - 81.25 MHz LDVS
  - 52.00 MHz 0 dBm
  - 50.00 MHz CMOS
  - 9.027 MHz TTL

- Phase accuracy and stability
  - RF station to RF station: 0.3° @ 1.3 GHz
  - Laser to 1st RF station: 0.2° @ 1.3 GHz

- The 0° phase reference point for 1300 MHz is the main 1300 MHz RF output on the master oscillator.

d. **Summary table**

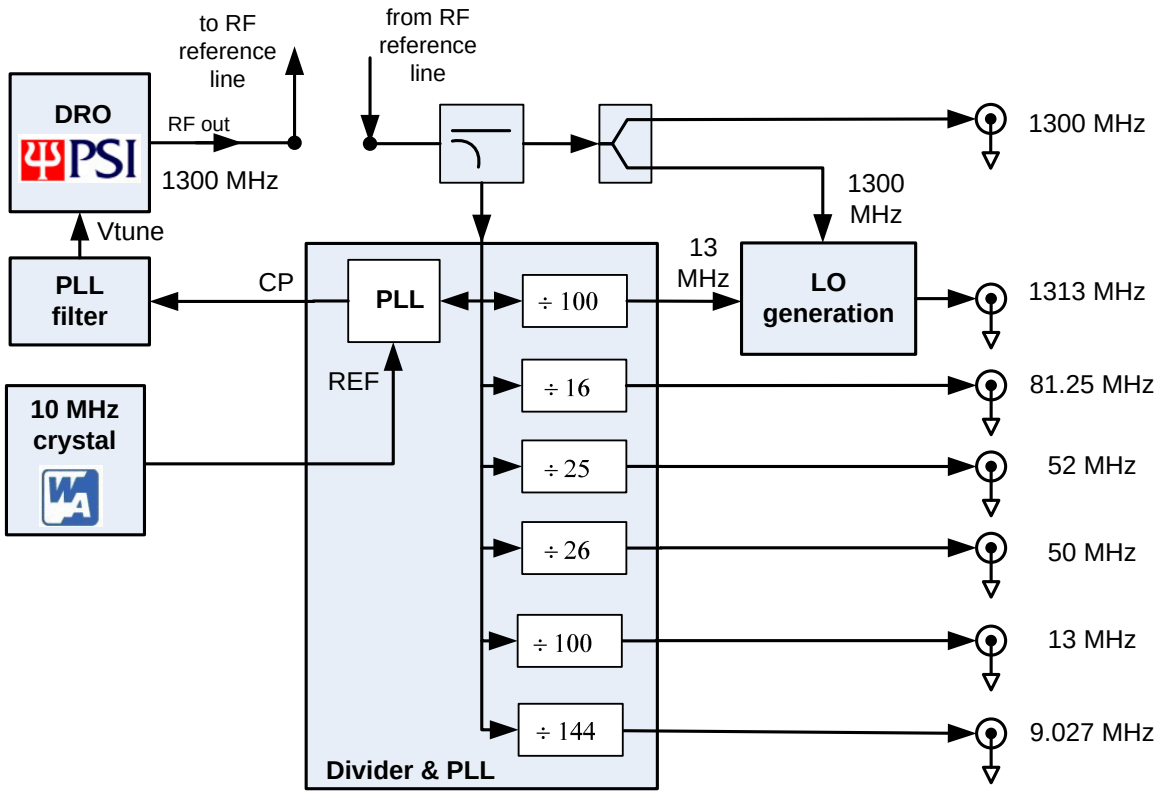
All specifications are summarized in the table below

Frequency	Description	Clients	Power level	Phase noise
1313 MHz	LO reference	LO distribution system	+10 dBm	
		RF receivers	+10 dBm	
		RF transmitter	+10 dBm	
		MFC controller clock	0 dBm	
1300 MHz	RF reference	RF distribution system	+10 dBm	
		RF receivers	+10 dBm	
		Instrumentation	0 dBm	
81.25 MHz	Laser reference	Laser	LVDS	
52.00 MHz	Piezo system LO	Cavity resonance control	0 dBm	
50.00 MHz	ESECON clock	ESECON controller clock	LVCMOS	
13.00 MHz	IF reference	Monitor system	0 dBm	
10.00 MHz	Crystal reference	Monitor system	0 dBm	
9.027 MHz	Timing reference	Timing system	TTL	

2. Block diagram

a. Simplified block diagram

The following block diagram shows the different subsystems of the master oscillator.



b. General description

The 1.3 GHz Dielectric Resonance Oscillator (DRO) is phase locked loop to the stable 10 MHz reference crystal. The 1.3 GHz is sent to the RF reference line system and brought back to the PLL from the end of the reference line, hence keeping a constant phase reference signal at the input of the divider block. All subsequent signals are divided down from the main 1.3 GHz reference inside the divider block. The local oscillator (LO) signal is generated by mixing the locked 1.3 GHz signal with a sub-harmonic intermediate frequency (IF) of 13 MHz, producing the 1313 MHz after filtering of the upper side band.

c. List of referenced schematics

More detailed schematics of the master oscillator subsystems are found here:

Y:\Projects\LLRF\Systems\NML\Documentation\Master Oscillator\

3. Design: subsystems

a. 10 MHz reference with electrical and mechanical tuner

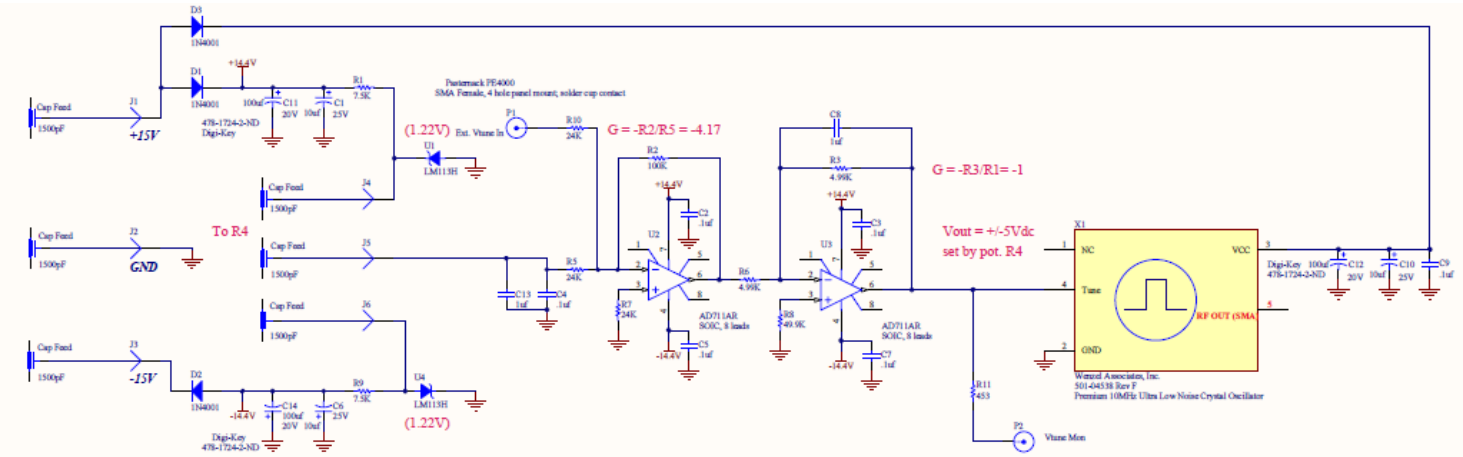
Description:

A voltage control oscillator provides a 10 MHz reference signal. This frequency can be adjusted mechanically and electrically.

Key features:

- Stable 10 MHz reference
- +12 dBm output level
- +/- 15VDC supply
- +/- 14 Hz mechanical tuning range
- +/- 3 Hz electrical tuning range
- RF tight casing
- Vibration proof support
- Electrical tuning monitor point
- Additional input to provide external electrical tuning

Block diagram:



Description of interface:

Inputs:

- +/- 15 VDC power supply
- External (5K) potentiometer 10 turns with lock for electrical tuning
- extra high impedance input (BNC) for electrical tuning
- opening in the casing for mechanical tuning

Outputs:

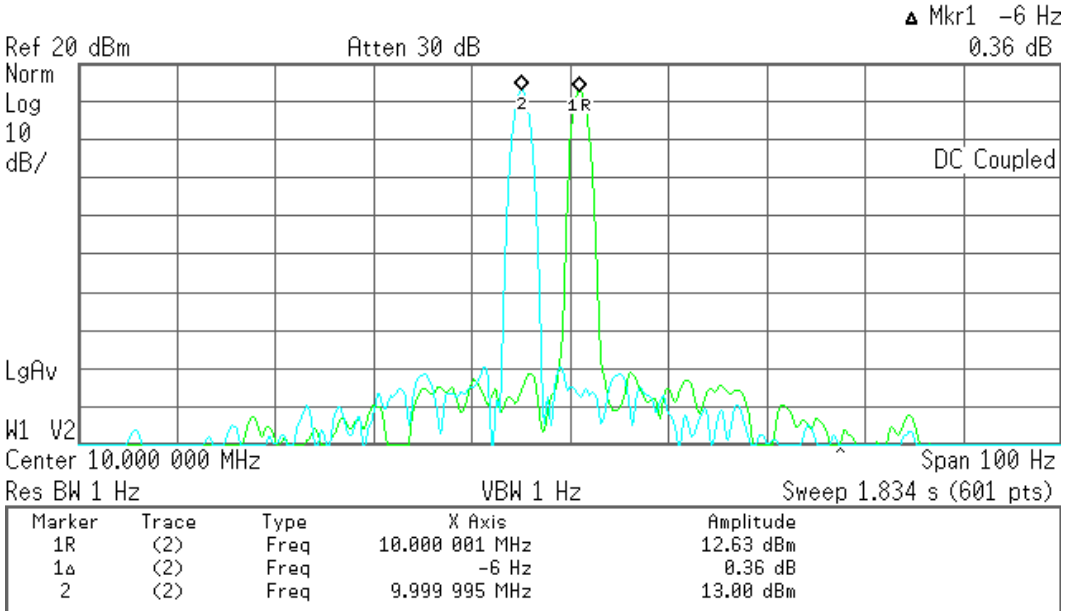
- 10 MHz RF main output (SMA)
- 10 MHz RF monitor output (SMA)
- Tuning voltage monitor point

Specifications:

Power Supply	nominal	units
	+15	V
first 3 minutes after 3 minutes	400 240	mA mA
	-15	V
	11	mA
Electrical tuning		
range	+/- 5 +/- 3	V Hz
sensitivity	$+/-2 \times 10^{-7}$	ppm
Mechanical tuning		
sensitivity	$+/-1 \times 10^{-6}$	ppm
range	+/- 14	Hz
Ouputs		
Main RF output level	+13	dBm
RF monitor	-10	dBm

Measurements:

Testing Crystal serial # 14075-0545
Electrical tuning range: 6 Hz



Using frequency counter: 9,999,995.062 Hz – 10,000,001.073 Hz

Notes:

Related documents:

Tuneable 10MHz Reference.pdf

C:\My documents\CC2\Master Oscillator\10 MHz crystal VCO\schematic\

b. Clock configuration circuit board

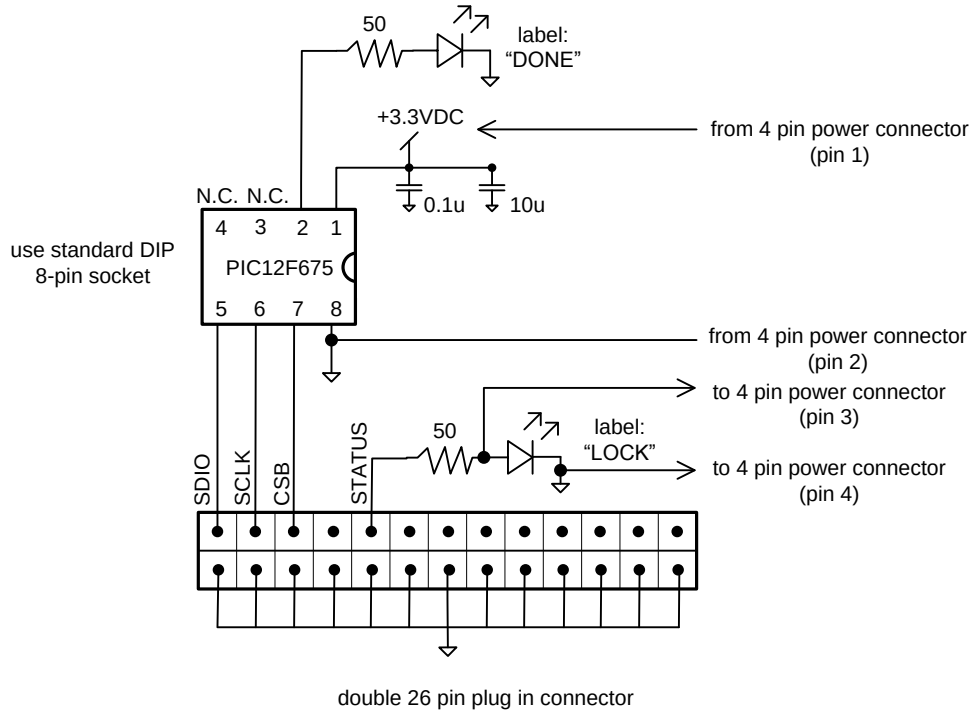
Description:

This board configures the clock chip of the AD9510 evaluation board. The configuration is performed by a PIC microcontroller. This configuration board is connected to the evaluation through a 26 pin header. The board gets its power from the AD9510 evaluation board. The programming is done using the chip serial port.
The board has a LED indicating when the programming is done. An output header is reserved for another LED indicating when the clock is locked to the reference signal.

Key features:

- Gets power from evaluation board
- Programming done LED indicator
- PLL locked LED indicator
- Programs directly upon boot up

Block diagram:



Description of interface:

Inputs (trough the 26 pin header):

- SDIO, pin 2 (serial I/O, not currently used)
- SCLK, pin4 (serial clock, used to clock the serial communication)
- CSB, pin 6 (chip select bar, used to gate individual communication cycles)
- SDO, pin 8 (serial output, used to write configuration to the clock)
- Status, pin 10 (soft tied to PLL status, un/locked, connected to output LED)
- Function, pin 12 (not currently used)
- VDD, pin 16, 3.3VDC from AD9510 eval board

Outputs:

- LED indicator for end of programming (on board)
- 2 pin header for front panel LED to indicate PLL lock status

Specifications:

Power Supply		
	+3.3	VDC
	<200	mA

Related files:

- PIC board_sch.pdf *schematic of the clock configuration board*
- PIC board_layout.pdf *silk screen layout of the clock configuration board*
- PIC12f675.pdf *documentation for the PIC microcontroller*

c. Phase lock loop filter

This section presents the design and measurements for the loop filter used in the phase lock loop.

Features:

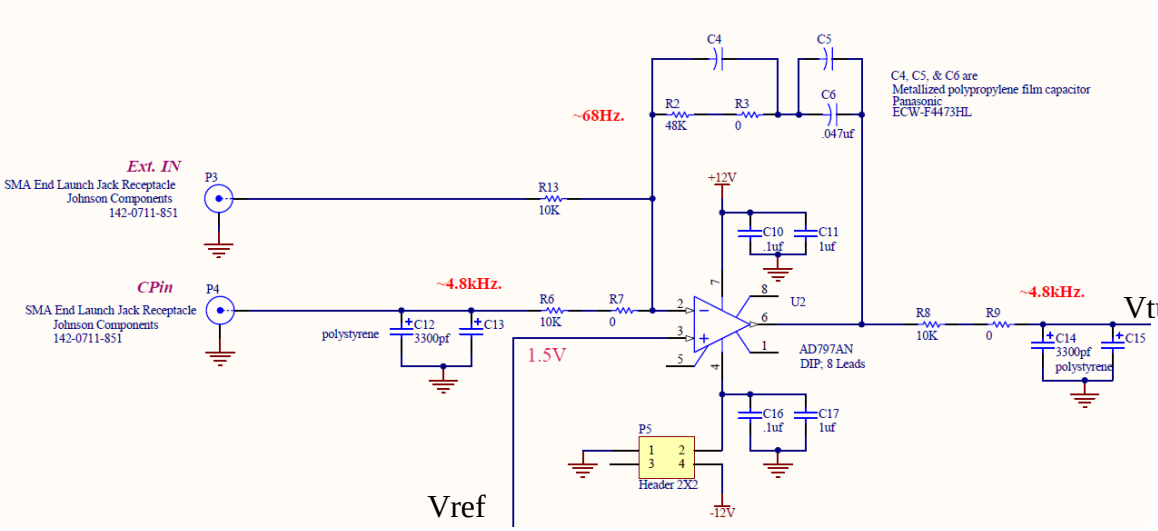
- low pass filtering of the charge pump current output of the PLL
- maximum voltage swing to optimize control of the DRO
- option to inject noise externally into the loop for noise analysis
- control voltage buffered monitor point available

Specifications:

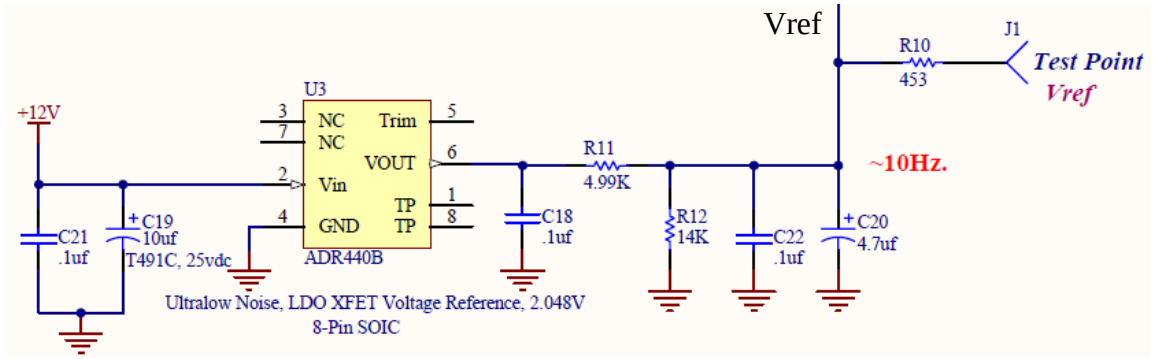
- Loop bandwidth: 500 Hz
- Phase margin: 70°
- Active filter design

Schematics:

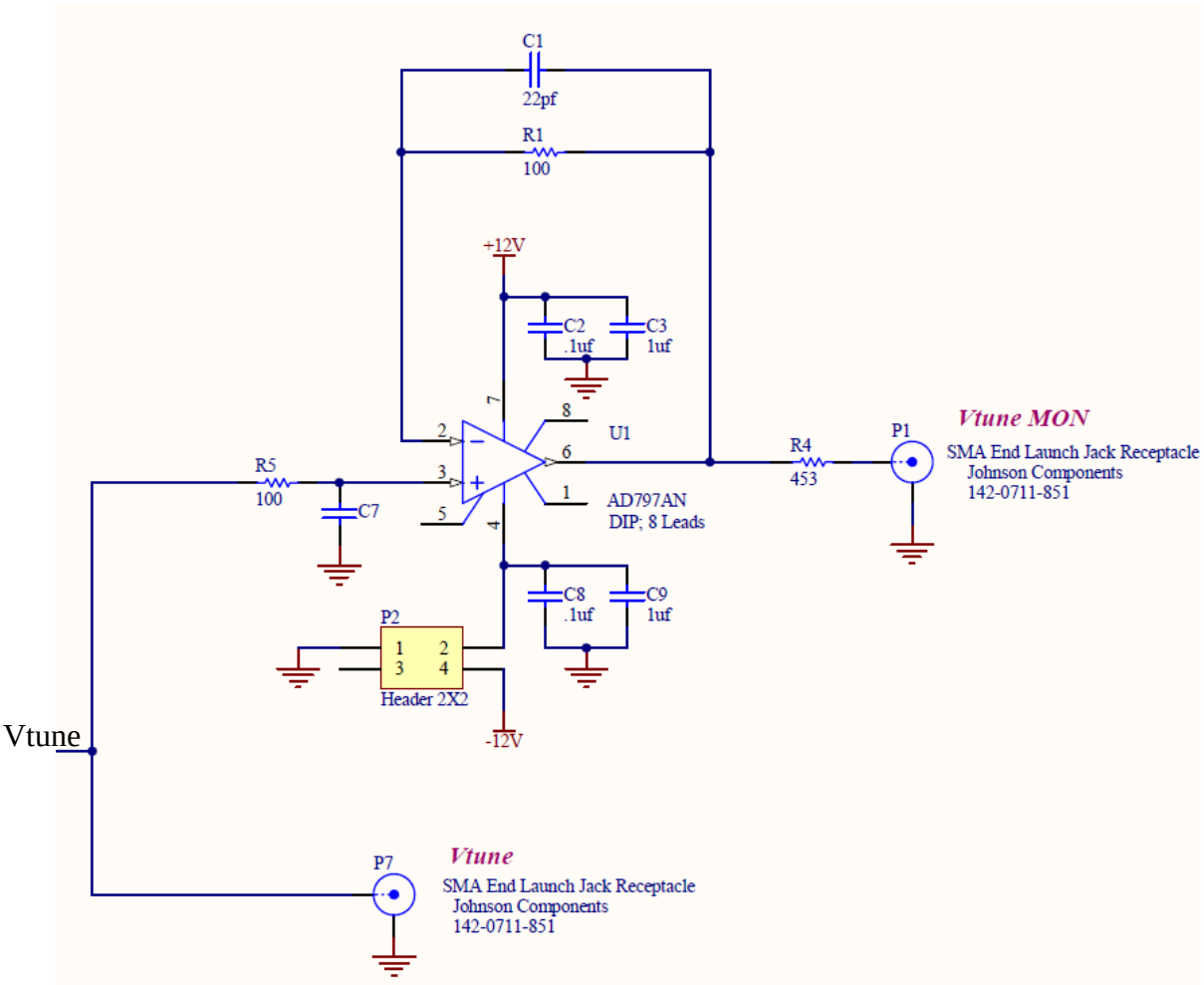
Loop filter section:



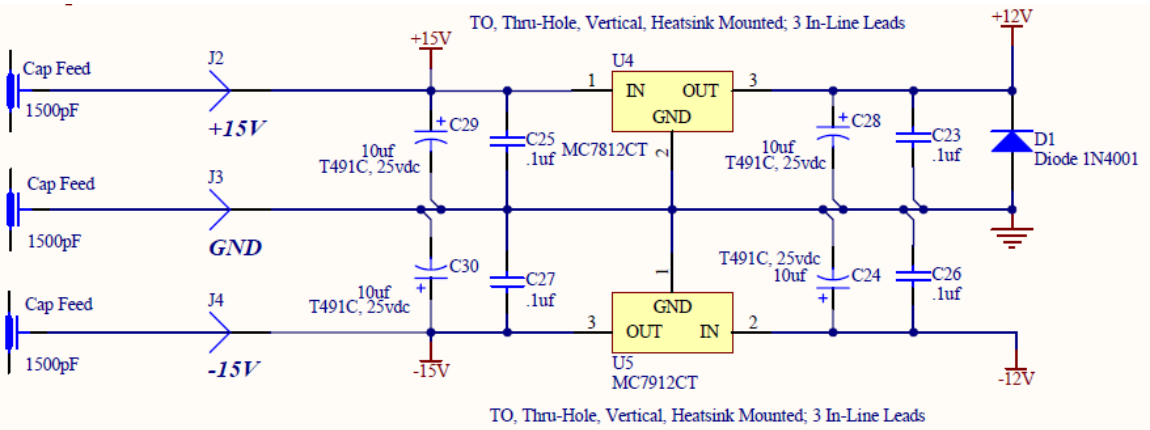
Voltage reference section:



Monitor point section:



Power regulation section:



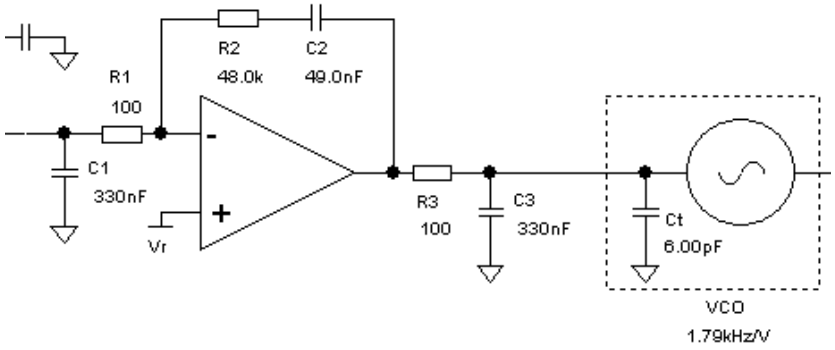
Design description:

Design using ADIsimCLK:

C:\My documents\CC2\Master Oscillator\ADIsimCLK\loop filter\filter_5.clk

Specifications:

Loop bandwidth ~500 Hz
Phase margin ~70 deg
Active filter design, 2 poles 1 zeros, with an OP27



The first pole (R1,C1) and the second poles (R3,C3) are at 4.8 kHz, the zero is (R2,C2) is at 68 Hz. The DC gain is G = –(R2/R1) = -480

In an alternate design, the values R1 and C1 are changed to R1=10k and C1=3.3nF. The pole remains the same, but the low frequency gain is dropped to G=4.8

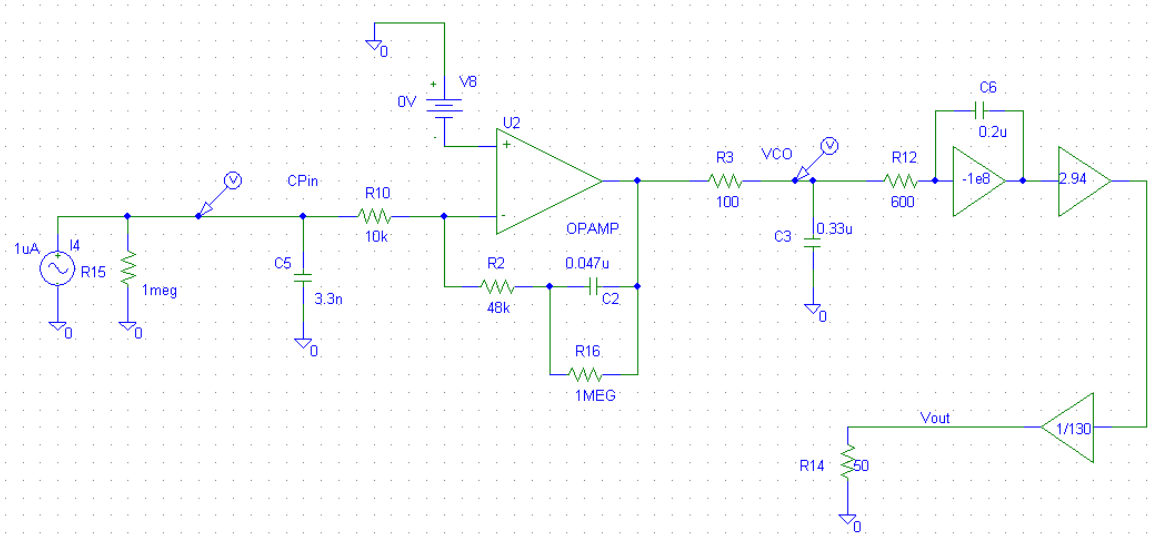
The reference voltage Vref is given by the low noise voltage reference chip ADR440B, providing 2.048V. A voltage divider 5K,14K brings the reference voltage down to 1.5V

Noise analysis:

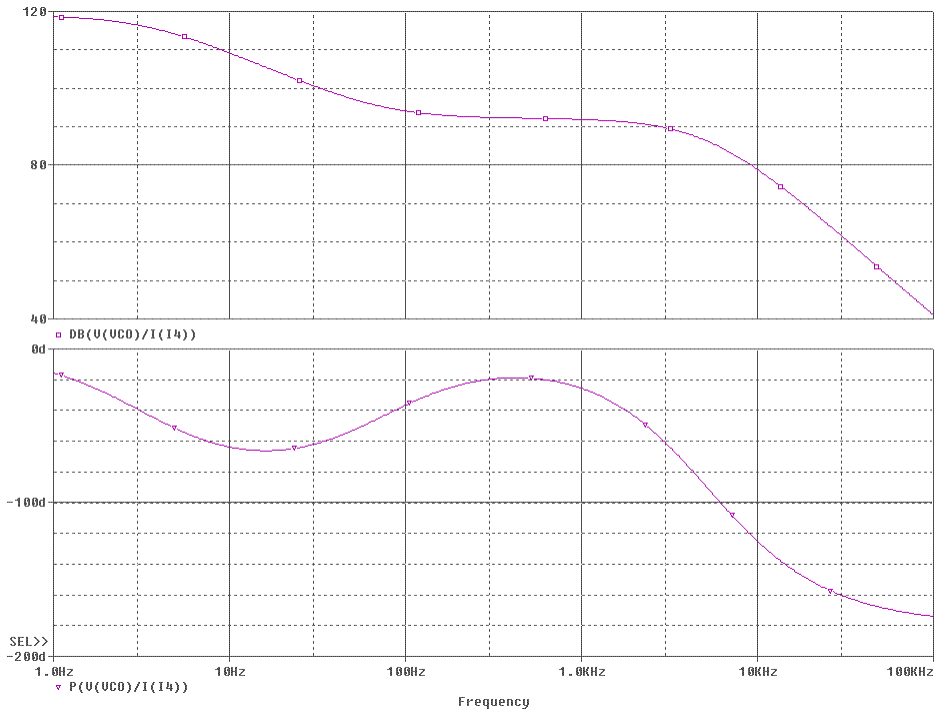
PSpice simulation: (design#5)

C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\PLL loop filter\PSpice

Schematic:

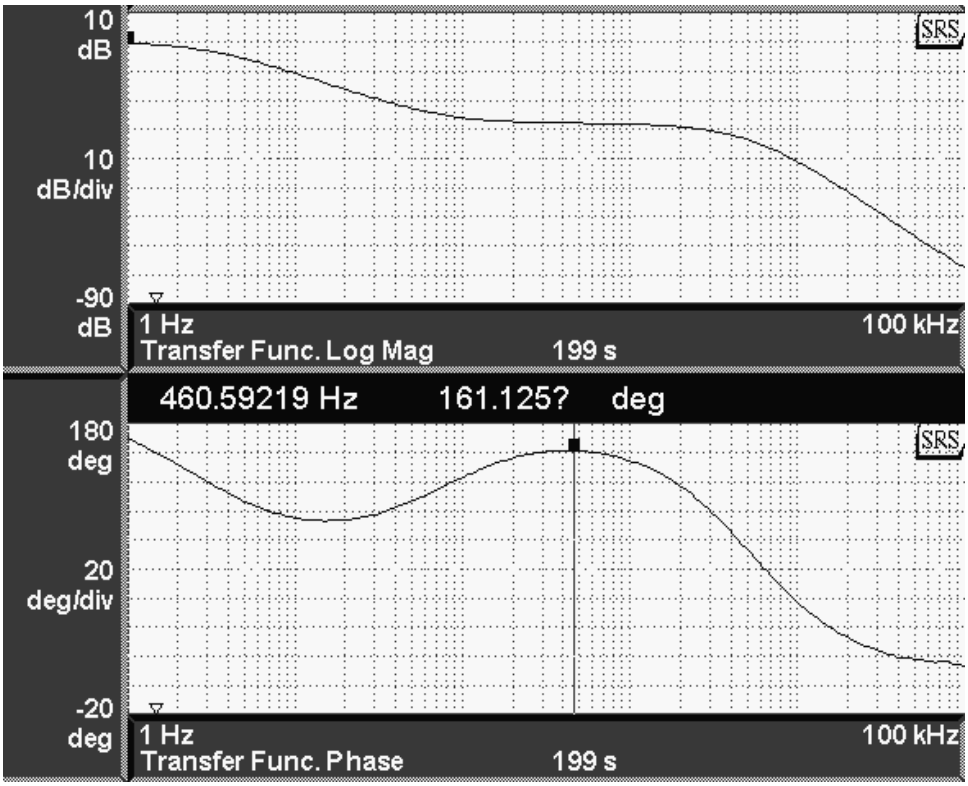


Transfer function:



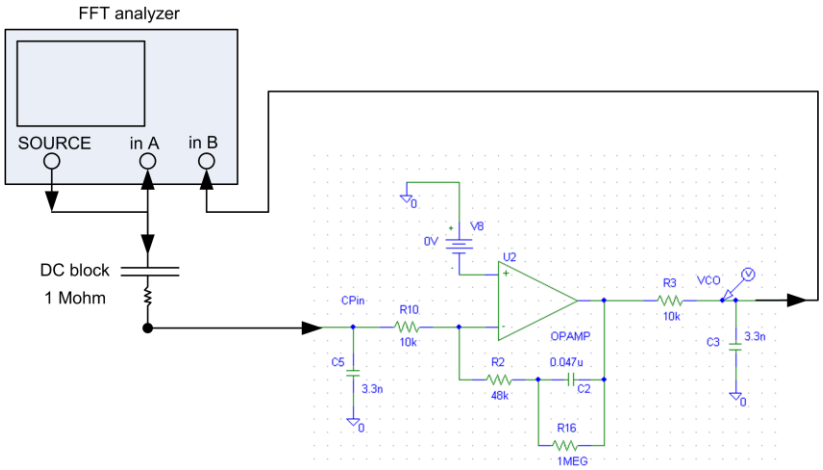
Measured transfer function:

C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\PLL loop filter\design#5



To measure the transfer function using the low frequency vector analyzer, a series resistor of 1 Mohm was put in parallel with the capacitor of the op amp feedback loop, to allow for DC current feedback. A DC block was also put in series with the analyzer's source and a 1 Mohm series resistor to make the source look like a current source.

Measurement setup:



Instrument setup:

Display setup:
Measure groups → Swept sine
Measurement → Transfer function
Freq.
Start → 1 Hz
Stop → 10 kHz
Type → log
points → 200
Display options
Format → Dual
Active display to toggle between top and bottom
Display setup (active A ; active B)
View → Log Mag
View → Phase

Interpretation of the two plots:

Looking at the phase, we can see the first pole around 3Hz. This is due to the 1 Mohm resistor in parallel with the 0.049uF capacitor.
The first zero appears around 70 Hz. It is due to the 48k resistor in series with the 0.049uF capacitor.
Then the second pole appears around 4.8kHz, it is due to the 100 ohms with the 0.33uF capacitor.
These features are observed on both plots.
The phase scale is off by 180 degrees comparing the simulation and the measured data. This is probably do to the fact that the gain is actually negative (sign inversion).
Looking at the amplitude plot, we also observe the 2 poles and the zero at similar frequency values. The difference in gain can be accounted for by the fact that in the measurement, a 1 Mohm resistor is placed in series at the CP input to emulate the current source behavior of the charge pump. This decreases the DC gain by roughly 10^6 or 120 dB.

Notes:

Related documents:
Schematic and PCB layout:

- PLL bot.pdf
- PLL top.pdf
- PLL Loop Filter.pdf
- PLL Loop FilterPCB.pdf

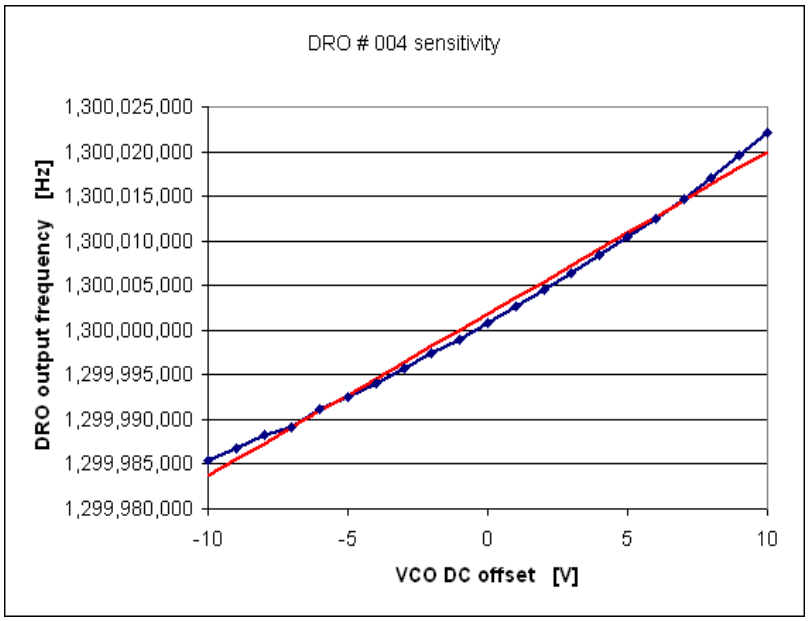
C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\PLL loop filter\Board layout

Components:

DRO:

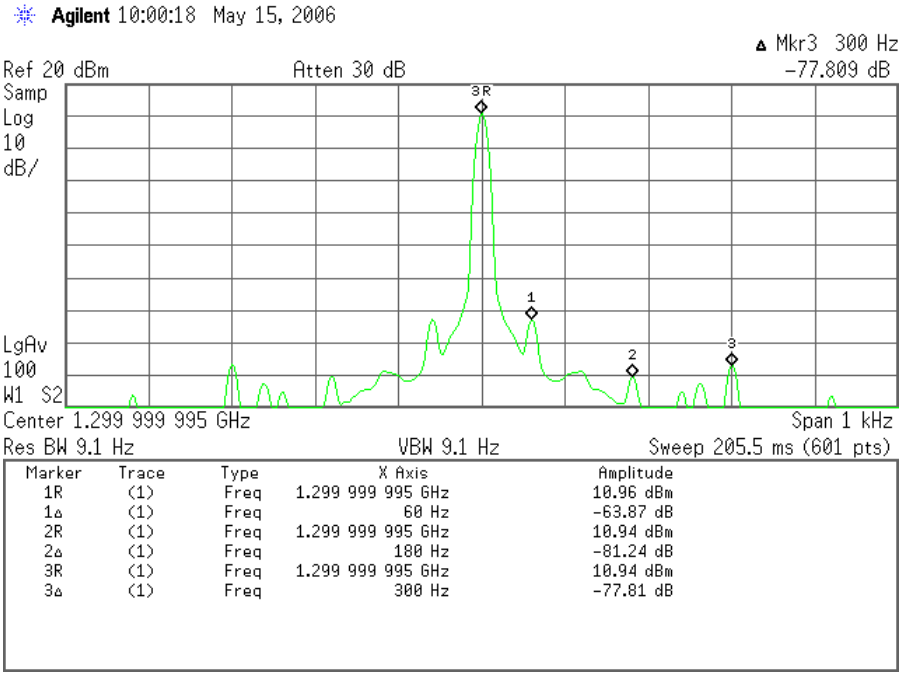
Sensitivity: DRO_sensitvity.xls in C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\DRO\

VCO [V]	Frequency [Hz]	Linear fit [Hz]
-10	1,299,985,445	1,299,983,692
-9	1,299,986,790	1,299,985,506
-8	1,299,988,230	1,299,987,320
-7	1,299,989,090	1,299,989,133
-6	1,299,991,090	1,299,990,947
-5	1,299,992,590	1,299,992,761
-4	1,299,994,012	1,299,994,575
-3	1,299,995,697	1,299,996,389
-2	1,299,997,367	1,299,998,202
-1	1,299,998,970	1,300,000,016
0	1,300,000,869	1,300,001,830
1	1,300,002,674	1,300,003,644
2	1,300,004,487	1,300,005,458
3	1,300,006,377	1,300,007,272
4	1,300,008,438	1,300,009,085
5	1,300,010,458	1,300,010,899
6	1,300,012,484	1,300,012,713
7	1,300,014,604	1,300,014,527
8	1,300,017,000	1,300,016,341
9	1,300,019,560	1,300,018,154
10	1,300,022,200	1,300,019,968

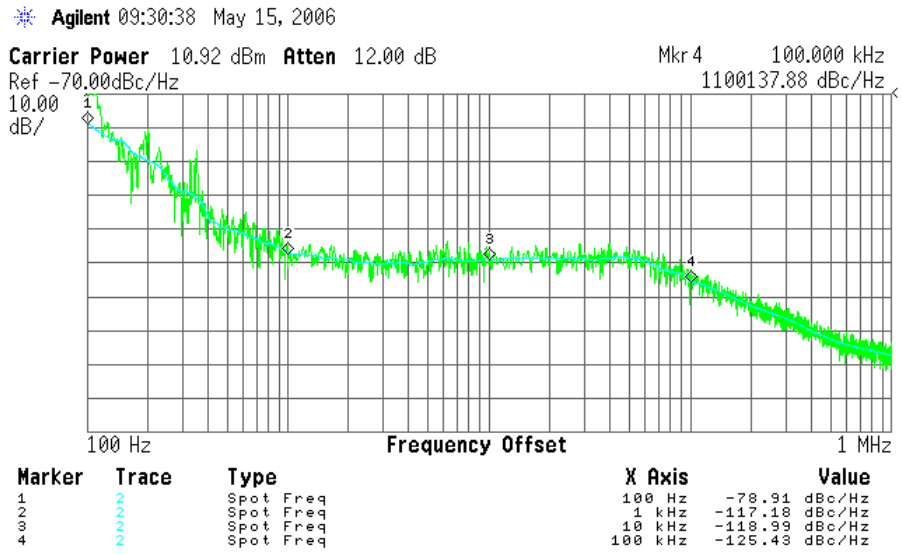


Kv =	**1,814**	**Hz/V**
Offset =	**1,300,001,830**	**Hz**

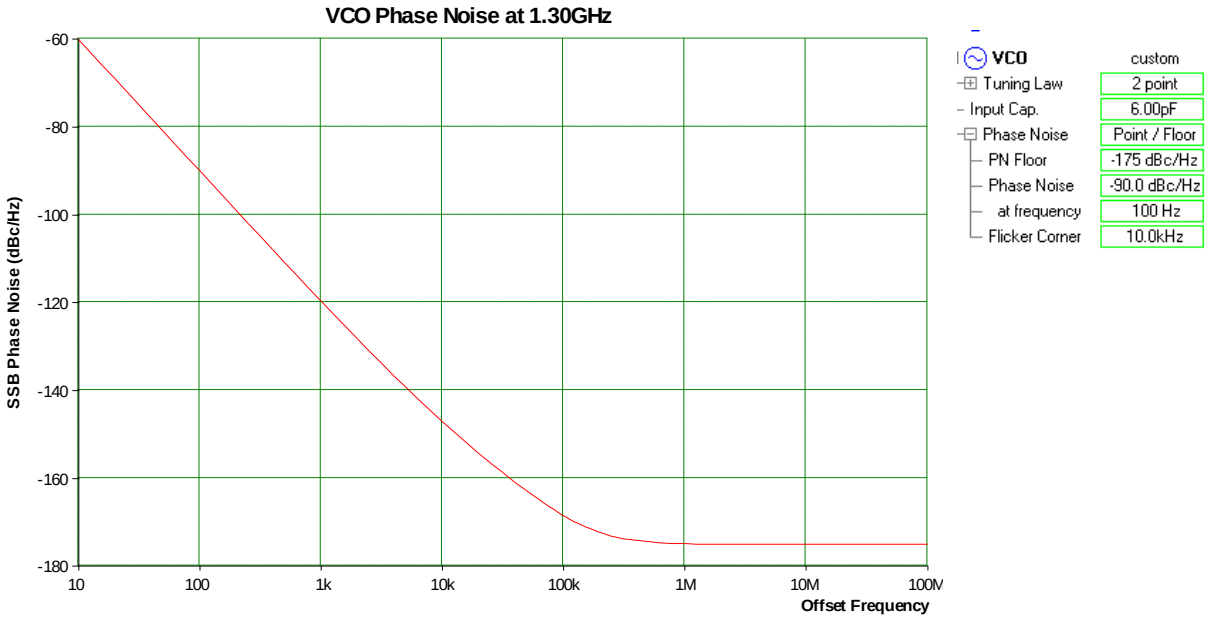
Narrow band spectrum: SCREN411.GIF in
C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\DRO



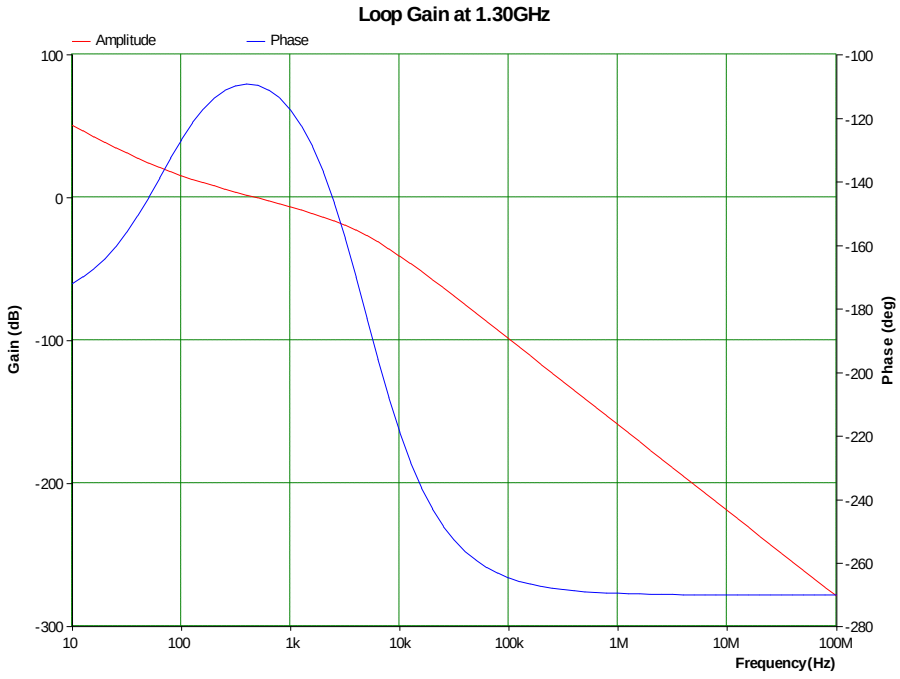
Phase noise: SCREN412.GIF in
C:\Documents and Settings\branlard\My Documents\CC2\Master oscillator\DRO



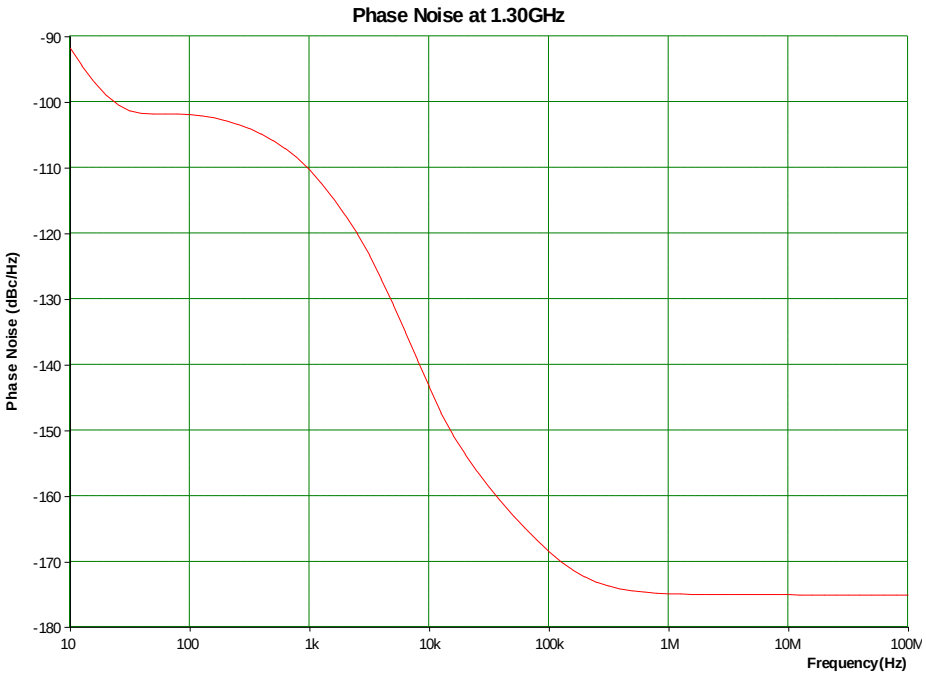
Phase noise values entered in ADIsimCLK for simulation



Expected closed loop gain and phase (ADIsimCLK)

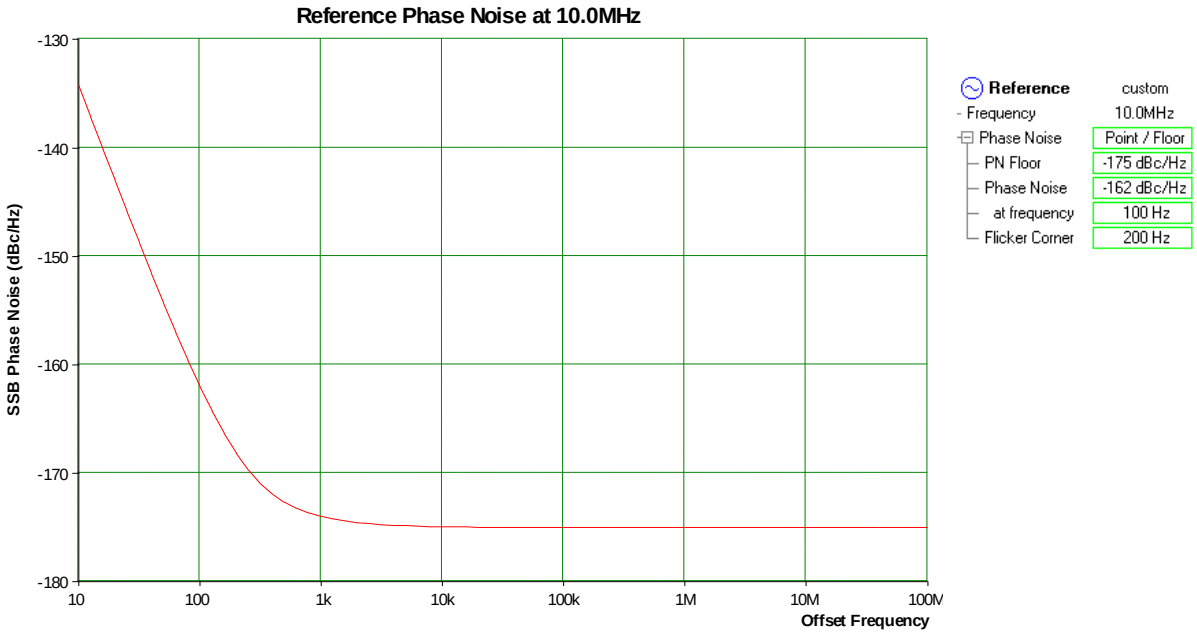


Expected phase noise at 1.3 GHz (ADIsimCLK)



COMPONENTS: 10 MHz reference:

Phase noise: (ADIsimCLK)



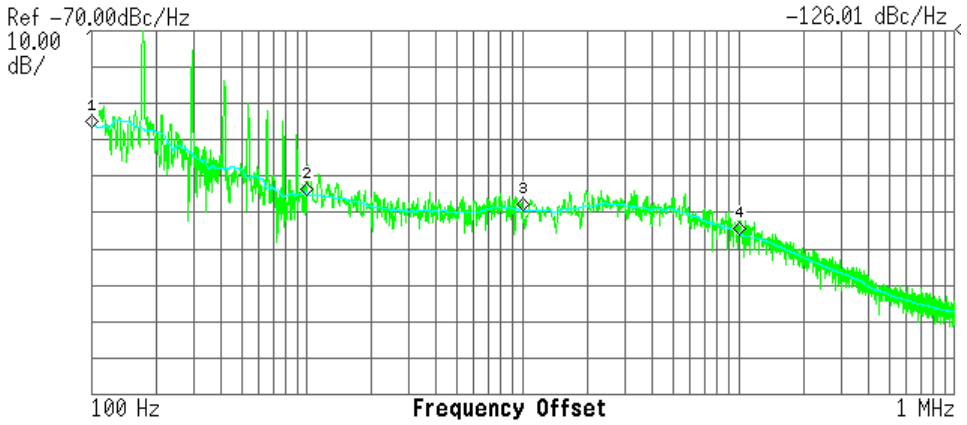
d. **Power supply**

The master oscillator has the following power consumption:

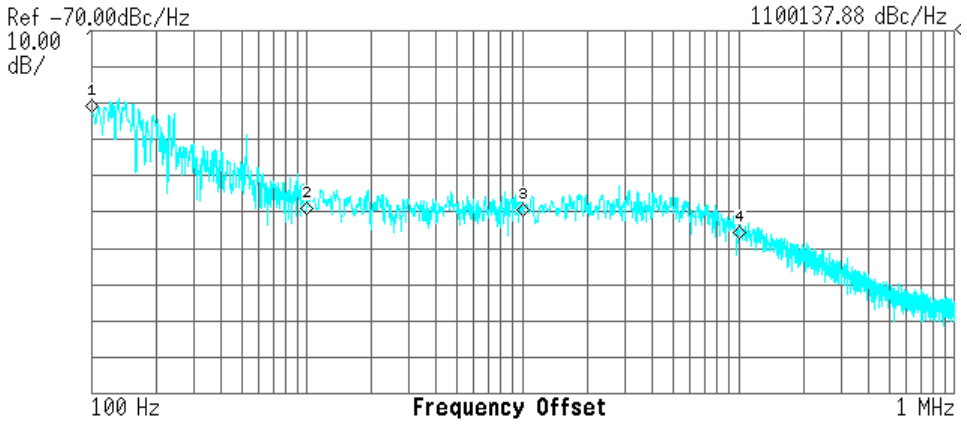
- +15 VDC, 1.5 Amp
- -15 VDC, 0.5 Amp
- +5VDC, 2.5 Amp

An external power supply was design to cover these needs, along with providing power for 2 up/down converters (each requiring +6VDC, 1.7 Amp and -6VDC, 0.5 Amp). Placing the power supply in an external chassis proved to be an efficient way to isolate the DRO from the line harmonics as illustrated in the 2 plots below:

Power supply in the master oscillator chassis:



Power supply in an external chassis:



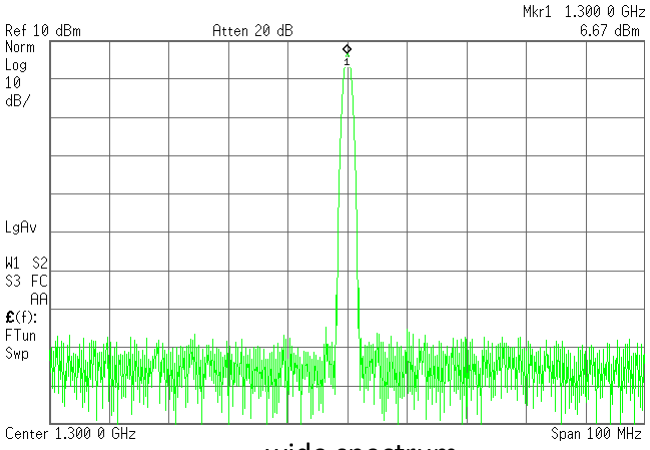
The complete power supply schematic can be found at this location:

Y:\Projects\LLRF\Systems\NML\Documentation\Master Oscillator\

4. Performance

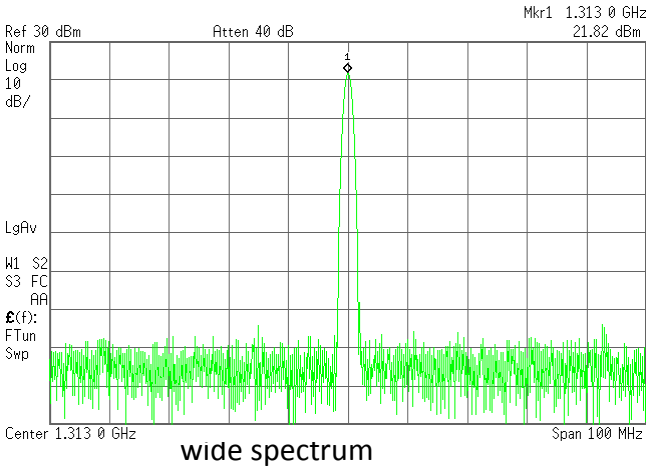
a. RF output spectrums

1300 MHz

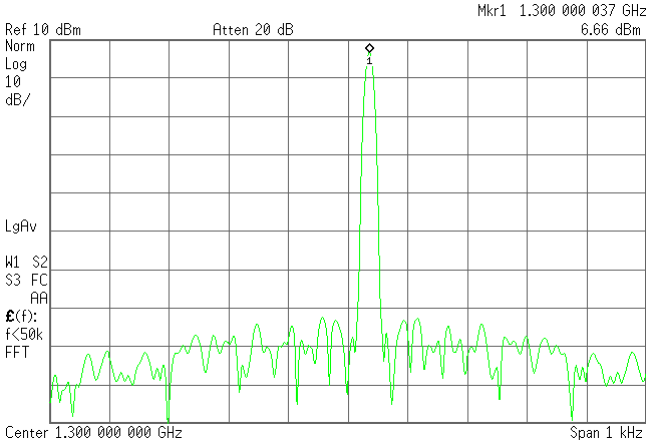


wide spectrum

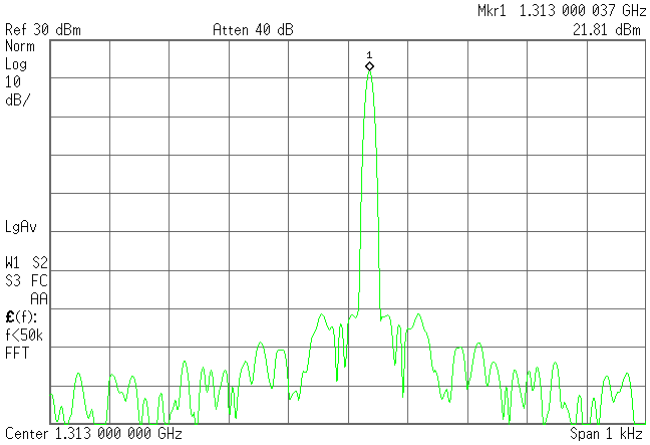
1313 MHz



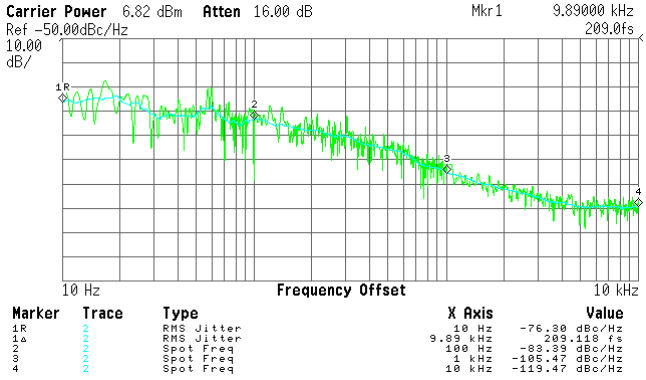
wide spectrum



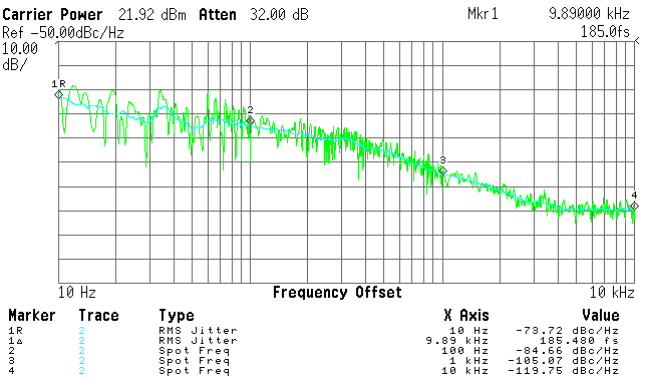
narrow spectrum



narrow spectrum



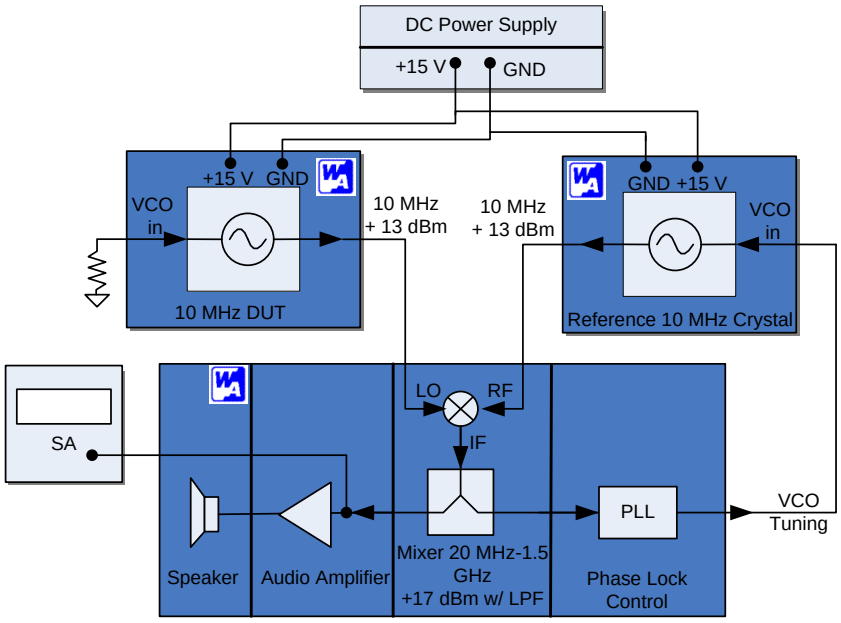
phase noise and integrated jitter



phase noise and integrated jitter

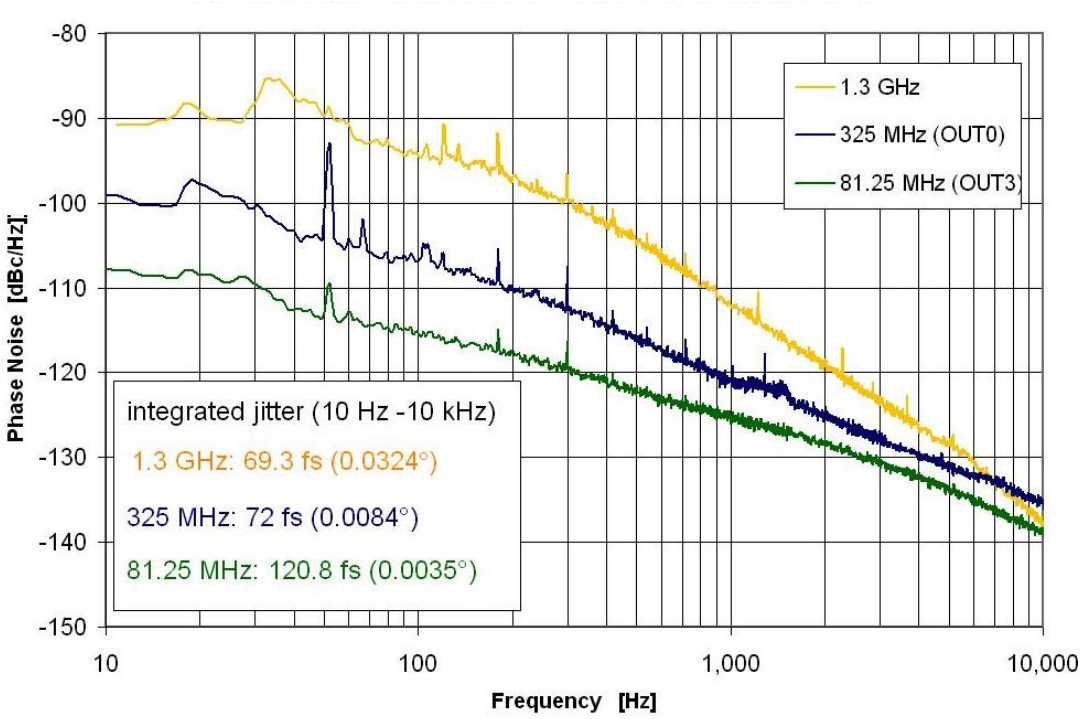
b. **RF phase noise measurements**

To perform an absolute phase analysis measurement, the following setup is used:



BluePhase 1000 Noise Analyzer

The plot below shows the phase noise spectrum for 1.3 GHz, 325 MHz and 81.25 MHz

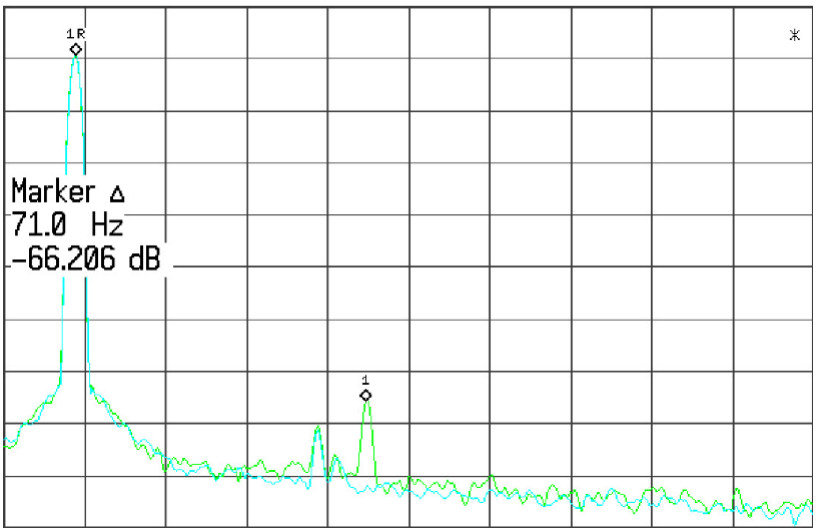


c. Study about isolation from microphonics

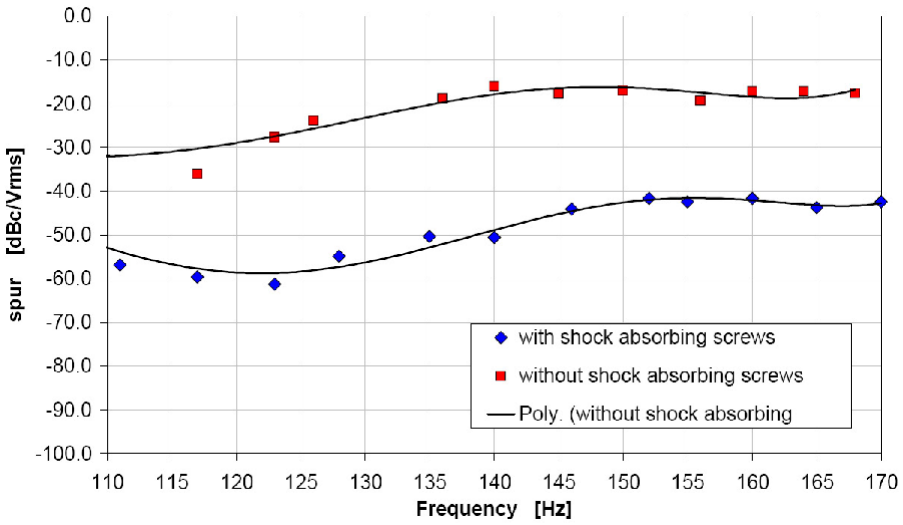
A mechanical analysis on the effect of microphonics vibrations on the master oscillator has been carried through and is reported in this document:

Beams-doc-3634:
"Study on Microphonics for the Master Oscillator Design at NML", J. Branlard, Aug. 2009

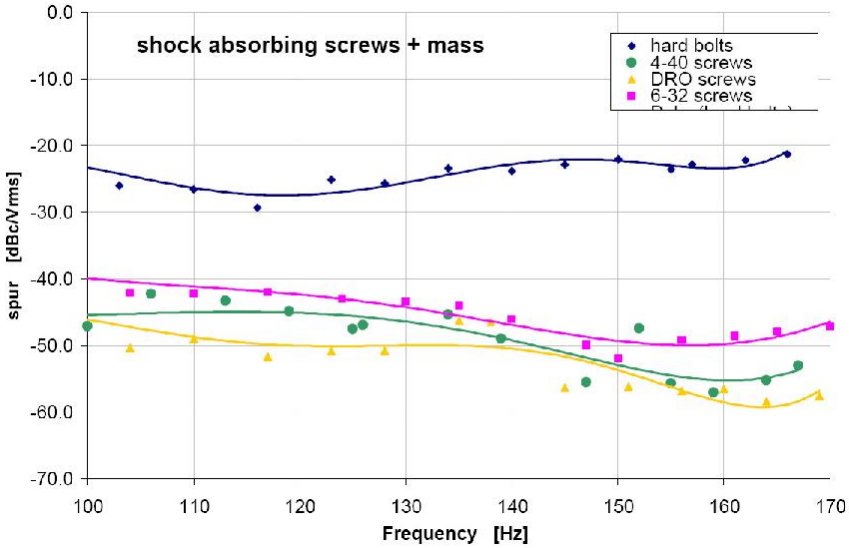
Some of the findings are summarized below.



Plot showing the 1.3 GHz signal with the microphonic stimulus ON and OFF:



Benefit of mounting the DRO on shock absorbing screws:



Comparative test between different shock absorbing screws: